Patent
Attorney's Docket No. 1032674-000200

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
Kevin M. Traynor et al.	Group Art Unit: 2111
Application No.: 10/626,756	Examiner: Justin King
Filed: July 24, 2003	Confirmation No.: 1739
For: METHOD AND SYSTEM FOR INTERRUPT MAPPING	

REQUEST FOR PRE-APPEAL BRIEF REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request review of the final rejections of claims 1-13 in the subject application. No amendments are being filed with this Request.

This Request is being filed with a Notice of Appeal.

Background

The claimed subject matter is summarized, with reference to the embodiment of Figure 3, in Applicant's response filed November 14, 2005, at pages 2-3. For purposes of this Request, claim 1 can be treated as a representative claim. It recites two steps, namely:

- mapping each of the plurality of interrupt sources (e.g. IS-01 to IS-K) to each of the plurality of interrupt inputs (INT-01 to INT-N); and
- selectively enabling interrupt requests from each of the plurality of interrupt sources to one or more of the plurality of interrupt inputs.

The rejections of claims 1-13 are based upon a combination of the Suh and Prenn patents.

Reasons for Request

1. The Disclosure of the Suh patent.

In making the rejection, the final Office Action refers to the parallel connection of the pending register 30 to each of the first priority determination logic 40 and the second determination priority logic 50 of the Suh patent. The structures of the first priority determination logic 40 and the second priority determination logic are the same (col. 5, lines 1-4), and illustrated in Figure 4 of that patent. The interrupt sources is0-is23 of first priority determination logic 40 have a one-to-one relationship to the inputs of the arbiter circuits 41-44. Interrupt sources is24 and is25 have a one-to-one relationship with two inputs of a fifth arbiter circuit 45. The same arrangement is present for the second priority determination logic.

At best, therefore, each interrupt source, e.g. is0, is mapped to at most two interrupt inputs, namely one input for the first priority determination logic and one input for the second priority determination logic. The Suh patent does not disclose that each of the plurality of interrupt sources is0 to is25 is mapped to "each" of the plurality of interrupt inputs, i.e. every one of the inputs for the first priority determination logic and/or every one of the inputs for the second priority determination logic.

2. Examiner's interpretation of the Suh patent.

In an interview conducted after the final Action, the Examiner suggested that the first priority determination logic 40 could be viewed collectively as one interrupt input and the second priority determination logic 50 could be viewed as a second interrupt input, thereby forming the claimed plurality of interrupt inputs as recited in claims 1 and 7. Applicants submit that a person of ordinary skill in the art would not

interpret the disclosure of the Suh patent in such a manner, relative to the claim language. As their names indicate, elements 40 and 50 of the Suh patent are logic circuits, as depicted in Figure 4. The interrupt inputs, i.e. the ports to which the interrupt signals are applied, comprise the individual input terminals of the logic circuit, not the circuits as a whole.

Nevertheless, even if the Examiner's interpretation is accepted, the references still fail to teach the claimed subject matter, as set forth below.

3. The Prenn patent does not cure deficiencies of the Suh patent or disclose all features of claims 1 and 7

The Prenn patent was cited as allegedly disclosing the claimed feature of selectively enabling interrupt requests from each of the plurality of interrupt sources to one or more of the plurality of interrupt inputs. The Office Action refers to Figure 6 and column 8, last paragraph through column 9, line 8 as disclosing a "PARTICIPATE" signal that allegedly selectively enables the associated interrupt signal. However, the "PARTICIPATE" signal has nothing to do with whether an interrupt source is connected to a given interrupt input.

Referring to Figure 2 of the Prenn patent, three interrupt sources are respectively associated with lines 116, 122 and 126. Their requests, labeled IA, IB and IC, are delivered to inputs of request logic 204, which generates the interrupt request signal IRQ. The PARTICIPATE signal does not selectively control the delivery of these requests to the inputs of the request logic 204. Rather, it is applied to a product term generator 252. As can be seen in Figure 2, this product term generator is associated with circuitry that is entirely distinct from the request logic 204. As such, the structure shown in Figure 6 is irrelevant to the claimed subject

matter. It has nothing to do with the connection of the lines 116, 122 and 126, i.e. the interrupt sources, to individual inputs of the request logic 204.

Consequently, the references fail to disclose the "selectively enabling" step of claim 1.

Conclusion

The Suh patent and the Prenn patent, individually or in combination, fail to disclose or suggest all of the features recited in the claims. As such, the Office Action does not meet at least one of the requirements for a prima facie case of obviousness. The record is not in a suitable posture for consideration by the Board of Appeals. Withdrawal of the final rejection is respectfully requested.

Respectfully submitted,

BUCHANAN INGERSOLL PC

Date: April 13, 2006

By: James Joel Zane, RN 28632
for Martin E. Miller
Registration No. 56,022

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620